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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C F R § 1 53(b))

Attorney Docket No.	503.37770X00
First Inventor or Application Identifier	Masahiko OGINO
Title	See 1 in Addendum
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

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2 [X] Specification [*Total Pages* 59]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 8]

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Addendum

1. SEMICONDUCTOR DEVICE, SEMICONDUCTOR WAFER, SEMICONDUCTOR MODULE, AND A METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE, SEMICONDUCTOR WAFER, SEMICONDUCTOR MODULE, AND A METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device comprising chip size package using for high density mounting module, multichip module, and the like, a method of manufacturing same, and to semiconductor wafer using for manufacturing the semiconductor device.

Currently, in accordance with making electronic devices small and high performance, semiconductor devices used therein are required to be high integration, high density, and fast in a processing velocity.

Corresponding to the requirement, implementing methods of semiconductor devices have been changed from pin insertion type to surface implementing method for increasing implementing density, and, in order to correspond to increasing the number of pins, packages such as from DIP (Dual Inline Package) to QFP (Quad Flat Package), PGA (Pin Grid Array), and the like have been developed.

However, implementation of the QFP is becoming difficult in accordance with increasing the number of pins, because connecting leads with implementing substrate are concentrated at periphery of the package, and the lead itself is thin and readily deformed. The PGA is disadvantageous in high density implementation, because

increasing processing velocity is difficult electrically, since terminals of the PGA for connecting with implementing substrate are slender and concentrated extremely each other, and surface implementation is impossible, since the PGA is a pin insertion type.

Recently, in order to solve the above problems and to realize a semiconductor device corresponding to increasing processing velocity, BGA (Ball Grid Array) has been developed. The BGA comprises a stress buffer layer between semiconductor chips and a substrate whereon circuits are formed, and bump electrodes, which are external terminals, at implementing substrate side of the substrate whereon circuits are formed (US Patent 5,148,265). The package having the BGA structure is readily implemented on surface, because deformation of the leads such as QFP is not occurred, since the terminals for connection with implementation substrate is ball-shaped solders, and a pitch between the terminals can be taken wide, since the terminals dispersed on all through the implementing plane. Furthermore, because the length of the bump electrode, i.e. the external terminal, is short in comparison with the PGA, inductance component is small, signal velocity is fast, and it is possible to correspond to the requirement to increase processing velocity.

On the other hand, JP-A-8-172,159 (1996) discloses LOC (Lead On Chip) package, which comprises a cross sectional composition of sealing material/chip/protecting film/sealing material, as the chip provided with the

protecting film. The protecting film increases adhesion of the chip with the sealing material, and protects the chip from damages by pick up pin, concurrently.

JP-A-7-135189 (1995) discloses an invention relating to wafer adhesion sheet for manufacturing semiconductor devices of LOC structure. The wafer adhesion sheet is sued as a protecting film until the chip is mounted in a package in a process for manufacturing the semiconductor.

Recently, in accordance with widespread used of portable information terminals, decreasing size and high density mounting of semiconductor devices are required. Therefore, CSP (Chip Scale Package), the package size of which is almost same as chip, has been developed. The CSP of various types are disclosed in "Nikkei Micro Device" p38-p64, published by Nikkei BP Co. (February, 1998). Those CSP are manufactured by the steps of: adhering semiconductor chips, which has been cut to respective pieces, onto a polyimide substrate or ceramic substrate, whereon circuit layer is formed; connecting electrically the circuit layer with the semiconductor chip by a method such as wire bonding, single point bonding, gag bonding, bump bonding, and others; sealing the connecting portion with resin; and forming external terminals such as solder bumps. JP-A-9-232256 (1997) and JP-A-10-27827 (1998) disclose methods of mass production of the CSP. In accordance with the methods, the semiconductor device is manufactured by the steps of: forming bumps on the semiconductor wafer; connecting the circuit substrate

electrically via the bumps; sealing the connecting portions with resin; forming the external electrodes on the circuit substrate; and cutting the wafer to respective pieces. The "Nikkei Micro Device" p164-p167, published by Nikkei BP Co. (April, 1998), discloses another mass production method of the CSP. In accordance with the disclosed method, the semiconductor device is manufactured by the steps of: forming bumps on the semiconductor wafer by soldering; sealing portions other than the bumps with resin; forming external electrodes at the bump portions; and cutting the wafer to respective pieces.

Among the above CSP assembled by adhering the semiconductor chips cut in pieces to the polyimide substrate or the ceramic substrate, the CSP, wherein the circuit layer is connected to the chip by wire bonding, becomes larger than the chip size, naturally, because the bonding area of the circuit layer is located at exterior of the chip. In case of the CSP connected by bump bonding, the substrate becomes larger than the chip in order to prevent resin from flowing down at potting, because the interval between the chip and the substrate is sealed with resin after bonding. Accordingly, there was such a problem that the package size of these CSP became larger than the chip.

The CSP using the chips cut in pieces had such a problem that the CSP took a long time in manufacturing the semiconductor device, because, after dicing the chips,

each of respective chip must be located correctly on the substrate, adhered thereon, connected electrically, and sealed.

The CSP using the resin substrate such as polyimide and the like as the circuit layer had such a problem that water, absorbed in the package at re-flowing when the package was provided onto the mounting substrate, was expanded and failures such as bubble formation and peeling off were generated, because the chip was adhered with an adhering agent.

The CSP, which was manufactured by the steps of: forming bumps on the semiconductor wafer; connecting the semiconductor wafer with the substrate; sealing the interval between the substrate and the semiconductor wafer with resin; forming the external electrodes; and cutting off the semiconductor wafer to respective pieces; had such a problem as warp of the semiconductor wafer and the semiconductor device by curing shrinkage, because the resin layer was formed only one side of the wafer.

Additionally, except the wire bonding type CSP, many of the CSP have an exposed plane, which is in reverse of the plane whereon the circuits are formed, of the chip. Therefore, there was a problem to generate failures such as cracks at edge of the chip, and damages at the rear plane by falling down during transportation of the package and handling such as picking up during mounting operation.

SUMMARY OF THE INVENTION

In consideration of the above circumstances, one of the objects of the present invention is to provide semiconductor devices and semiconductor wafer; wherein the package size is as same as the chip size, and failures in appearance such as warp and damages are scarcely generated; and to provide a method of manufacturing the same.

Other one of the objects of the present invention is to provide to provide semiconductor devices and semiconductor wafer; the package size of which is as same as the chip size, superior in mounting reliability and mass producibility, and failures in appearance such as warp and damages are scarcely generated; and to provide a method of manufacturing the same.

The gist of the present invention to achieve the above objects is featured by the semiconductor device comprising a semiconductor chip, a stress relaxing layer provided on the plane, whereon the circuit and electrodes are formed, of the semiconductor chip, a circuit layer formed on the stress relaxing layer and connected to the electrodes, and external terminals provided on the circuit layer; further comprises an organic protecting film provided on the plane contrary to the stress relaxing layer of the semiconductor chip.

Other feature of the present invention is in the semiconductor device comprising a semiconductor chip, a porous stress relaxing layer provided on the plane, whereon the circuit and electrodes are formed, of the semiconductor chip, a circuit layer formed on the stress relaxing layer

and connected to the electrodes, and external terminals provided on the circuit layer; further comprises an organic protecting film provided on the plane reverse to the stress relaxing layer of the semiconductor chip, and respective of side planes of the stress relaxing layer, the semiconductor chip, and the organic protecting film is exposed outside on a same plane.

Other feature of the present invention is in the semiconductor device comprising a semiconductor chip, a porous stress relaxing layer provided on the plane, whereon the circuit and electrodes are formed, of the semiconductor chip, a circuit layer formed on the stress relaxing layer and connected to the electrodes, an anisotropic conductor for electrical connection provided between the electrodes on the semiconductor chip and the circuit layer, external terminals provided at designated locations on the circuit layer in a grid array shape; and an organic protecting film provided on the plane reverse to the plane, whereon the circuit and the electrodes are mounted, of the semiconductor chip; wherein, respective of side planes of the stress relaxing layer, the semiconductor chip, and the organic protecting film is exposed outside on a same plane.

Other feature of the present invention is in the semiconductor wafer comprising plurality of chip areas, each of which comprises circuit and electrodes;, a stress relaxing layer provided on the plane, whereon the circuit and electrodes in the chip area are formed; a circuit layer

formed on the stress relaxing layer and connected to the electrodes; and external terminals provided on the circuit layer; further comprises an organic protecting film provided on the plane reverse to the stress relaxing layer in the chip area.

Other feature of the present invention is in the method for manufacturing semiconductor device comprising the steps of: forming the stress relaxing layer on the plane, whereon the circuit and electrodes are formed, of the respective chip area of the semiconductor wafer; forming an organic protecting film on the plane reverse to the plane, whereon the electrodes are formed, of the respective chip area; forming via-holes in the stress relaxing layer on the chip area; forming conductors in the via-holes; forming circuit on the stress relaxing layer; forming the external terminals on the circuit layer; and cutting the chip area, the substrate having the circuit, and the organic protecting film at the same plane so as to be minimum units for operating the semiconductor device obtained by the cutting.

On the semiconductor wafer disclosed in the present invention, plurality of chip areas are arranged regularly; the chip area is the minimum unit circuit for operating the semiconductor device, comprising semiconductor circuits such as logic, memory, gate array, and the others, and the electrodes for input/output of electric signals with outside the semiconductor wafer. The electrodes of the semiconductor device are arranged in a manner indicated

in FIG. 11.

In accordance with the present invention, the substrate provided with the circuit layer is composed of the porous stress relaxing layer and the circuit layer, whereon the circuits are formed. The porous body is composed of a body comprising a structure of continuous bubbles having many fine pores inside, or a three dimensional net work structure having breathing property. The porous body is formed by any one of: a track etching method, wherein the member is irradiated by neutrons and etched by a chemical agent; a drawing method, wherein crystalline polymer is heated or plasticized with a plasticizer, and subsequently, the crystalline polymer is drawn; a dissolution layer separating method, wherein a solvent having different solubility depending on temperature is used; an extraction method, wherein a polymer is mixed with an inorganic salt, silica, and others uniformly, and after forming a film, only the inorganic salt, and silica are extracted; a layer transferring method, wherein a polymer, a good solvent, and a poor solvent are mixed together, and after forming a film, only the good solvent is evaporated; and others. Additionally, non-woven fabric, a sheet of which is formed by a paper machine using polymers polymerized in a solvent in a fibrous state, is included. The breathing property means a phenomenon that a gas such as steam, air, and others passes through the porous body via fine pores existing inside the porous body.

In accordance with the present invention, the linear expansion coefficient of the protecting film is preferably close to the linear expansion coefficient of the adhesion layer for adhering the stress relaxing layer with the semiconductor chip. The warp of the semiconductor chip and the semiconductor wafer by thermal stress can be prevented by making the difference of the linear expansion coefficient of the organic protecting film from those of the stress relaxing layer and the adhesion layer small. Thickness of the protecting film is thicker than thickness of passivation film such as PIQ formed on the plane, whereon the circuits are formed, and thinner than the thickness of the chip. After back grinding the rear plane of the wafer, the protecting film can be formed by adhering a sheet of the protecting film to the back ground plane of the semiconductor wafer, or coating the plane with a varnish made of the protecting film material by spin coating method. The protecting film is adhered tightly to the wafer. The protecting film is desirably colored with black for shielding light.

In accordance with the present invention, the porous relaxing layer can be made of polycarbonate, polyester, aromatic polyester, polytetrafluoroethylene, polyethylene, polypropylene, polyvinylidene fluoride, cellulose acetate, polysulfone, polyacrylonitrile, polyamide, aromatic polyamide polyimide, aromatic polyimide, and their compounds. A part of the relaxing layer may be formed of a photosensitive material. The

relaxing layer is more porous than the protecting film.

The circuit layer can be formed with any of gold, copper, aluminum, and these conductors, the outer surface of which plated with gold. These circuit layer can be the insulating substrate, whereon the circuits are formed with one of these conductors. The insulating substrate is desirably made of engineering plastics superior in heat resistance and mechanical characteristics such as polyimide and the like.

The circuit layer is manufactured by forming the conductor layer directly on the relaxing layer by vapor deposition or plating and the like, and subsequently, forming the circuits by etching the conductor layer. Otherwise, the circuit layer can be formed by adhering the insulating substrate, whereon the circuit are formed with the conductor, onto the stress relaxing layer. The adhering agent is composed of any resin of epoxy, maleimide, phenol, cyanate, polyamide, polyimide, polyamide-imide, polyester, polyolefin, polyurethane, and the like, and a mixture of any of these resins with rubber component such as silicone rubber, nitrile-butadiene rubber, and the like. Additionally, any agent, which exerts an adhesion force by heating, drying, pressurizing, photo-irradiation, and others, can be used as the adhering agent. In addition to the above compounds, the adhering agent can be a sheet, which is formed by impregnating any of the above compounds into a core material such as porous body, glass cloth and the like.

The substrate, whereon the circuits are formed, is adhered to the semiconductor wafer with the above adhering agent.

The circuit layer is formed by the steps of: forming the porous relaxing layer on the electrode side plane of the semiconductor wafer; and forming the conductor layer on the relaxing layer by a method such as adhesion, plating, vapor deposition, and others. Sometimes, the circuit layer is formed by pattern-etching the conductor layer with a designated process.

The via-hole formed between the circuit layer and the semiconductor wafer is manufactured by laser such as He-Ne laser, Ar laser, YAG laser, carbon dioxide gas laser, and the like. Additionally, in some cases, the portions of the relaxing layer corresponding to the electrodes and the circuit layer of the semiconductor wafer are formed with a photosensitive material, and the via-hole is formed by exposing, developing, and etching of the photosensitive material.

The conductor portion for connecting electrically the semiconductor wafer and the circuit layer is formed with a conductive resin made by mixing conductive fine powder such as carbon, graphite powder, gold, silver, copper, nickel, copper plated with silver, glass plated with silver, and the like into a resin group binder such as epoxy group resin, silicone group resin, polyimide group resin, and the like. Electrical conduction can be achieved by forming a plated film in the via hole with metal such as copper by plating method. Additionally, the

conductive portion can be manufactured by forming a deposition film on the inner wall of the via-hole with metal such as gold, copper, and others by heating deposition or spattering deposition in vacuum. Other than the above method, in some case, the wafer is connected electrically with the circuit layer by arranging a material having anisotropic conduction in a direction of thickness between the semiconductor wafer and the terminals of the circuit layer. The material having anisotropic conduction is such a material manufactured by forming through holes with 20 - 30 μm pitch in an insulation film such as polyimide and the like, and filling the through holes with a conductive material such as copper and the like. The material is conductive only when the electrode exists at the same position in the thickness direction, and not conductive in the XY direction.

The external electrode to be formed on the substrate, whereon the circuit layer is formed, is a conductor connecting electrically the semiconductor device by melting with heating. Practically, any of a soldering alloy containing tin, zinc, and lead, silver, copper, or gold, or these metals formed in a ball shape and coated with gold, can be used for connecting the semiconductor device by heating and melting, or contacting and vibrating without melting. Other than these material, any one of molybdenum, nickel, copper, platinum, titanium, and others, or an alloy composed of at least two of these elements, or a double film structure formed by at least

two of these elements, can be used as the terminal.

The mounting substrate used for the semiconductor module is composed of the conductive layer and the insulating layer. The insulating layer is composed of resin such as epoxy, maleimide, phenol, cyanate, polyamide, polyimide, polyamide-imide, polytetrafluoroethylene, and the like, a copolymer of these resin, or a rubber component such as silicone rubber, nitrile-butadiene rubber, and the like. In particular, one of the above resin added with photosensitivity, which can be made patterning by a process such as exposing and developing, is preferable. Furthermore, in addition to the above resin itself, the insulating layer can be formed by impregnating any of the above compounds into a core material such as porous body, glass cloth and the like.

The conductive layer is composed of metal such as gold, copper, aluminum, and the like. In consideration of electrical characteristics, the mounting substrate is desirably a substrate, whereon a ground layer and a power supply layer are provided.

In accordance with the present invention, the CSP having a package size as same as the chip size can be provided. The porous stress relaxing layer is used. The porous body is cut simultaneously when the semiconductor wafer is cut. Its end plane is inevitably exposed at side plane of the package. Therefore, absorbed moisture at reflowing in mounting is released outside passing through the porous body. Accordingly, failures such as peeling off by vapor

pressure of water can be prevented , and the CSP having a high reliability can be provided. Because the wafer is cut altogether to pieces of respective unit after assembling by wafer level, the CSP having a preferable mass producibility can be provided. Furthermore, the CSP, wherein the warp generated by thermal stress is made small by the protecting film formed on rear plane of the semiconductor wafer, and appearance failures such as cracks and damages of the semiconductor chip during handling the package such as transportation and others is scarcely generated, can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a set of schematic cross sections indicating manufacturing steps of the semiconductor device in one of the embodiment of the present invention,

FIG. 2 is a perspective view of the semiconductor wafer based on the present invention obtained by the manufacturing steps indicated in FIG. 1,

FIG. 3 is a set of schematic cross sections indicating manufacturing steps of the semiconductor device in the other embodiment of the present invention,

FIG. 4 indicates an example of semiconductor device in the other embodiment of the present invention, and indicates (a) a schematic cross section, and (b) a perspective view,

FIG. 5 indicates an example of semiconductor device in the other embodiment of the present invention, and

indicates (a) a schematic cross section, and (b) a perspective view,

FIG. 6 is a set of perspective views indicating a part of manufacturing steps of the semiconductor device in the other embodiment of the present invention,

FIG. 7 indicates an example of semiconductor module based on the present invention, and indicates (a) a schematic cross section, and (b) a perspective view,

FIG. 8 is a schematic cross section indicating an example of semiconductor device of a comparative example,

FIG. 9 is a schematic cross section indicating an example of semiconductor device of a comparative example,

FIG. 10 is a schematic cross section indicating an example of semiconductor device of a comparative example, and

FIG. 11 is a schematic illustration indicating the arrangement of electrodes on the semiconductor chip used in the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Hereinafter, embodiments of the present invention are explained in detail referring to drawings.

(Embodiment 1)

FIG. 1 indicates manufacturing steps of semiconductor device in an embodiment of the present invention, and a semiconductor device obtained by the manufacturing steps.

In accordance with the manufacturing steps of (a) ~

(i), the semiconductor wafer and the semiconductor device of the present invention were prepared.

(a) As the insulating substrate 1, polyimide film (UB rex S: made by Ube Kosan Co.) of 50 μm thick, whereon an epoxy group adhesive agent was applied, was used. Device holes were formed by punching the insulating substrate 1. Electrolytic copper foil of 18 μm thick was adhered to the polyimide film by heating and pressurizing with a roller at 150 ℃. After applying photosensitive resist (P-RS300S: made by Tokyo Ohka Co.)onto the electrolytic copper foil, baked at 90 ℃ for 30 minutes, and the etching mask was prepared by exposing and developing the pattern.

Then, the copper was etched with ferric chloride aqueous solution (ferric chloride concentration is 40° Baume: specific gravity; approximately 1.38) at 40 ℃, and copper circuit was prepared by peeling off the resist. The circuit 2 was prepared by plating the circuit portion with electrolytic gold. As explained above, the circuit 2 corresponding to respective of plural chip areas on the semiconductor wafer was prepared.

(b) An adhesive varnish containing non-volatile component 30 % (bisphenol A type epoxy resin (EP1010: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone, ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.) was mixed) was applied onto one of surfaces of the porous body 3; composed of polyimide non-woven cloth having three

dimensional network structure of 150 μm; and dried the varnish. By adhering the circuit layer 2 prepared by the manufacturing step (a) to the porous body 3 via the adhesive agent by heating and pressurizing at 120 ℃ for 5 seconds, the substrate comprising the circuit layer was prepared.

(c) The substrate, whereon the circuit layer was formed, the adhesive agent 4, the semiconductor wafer 6, and the wafer protecting film 7 were arranged as indicated in FIG. 1. The substrate 1, whereon the circuit layer was formed, and the electrode 5 on the wafer were adjusted their position to match each other. As the semiconductor wafer 6, a semiconductor wafer of 4 inches and 525 μm thick was used.

The adhesive agent 4 and the wafer protecting film 7 were prepared by impregnating the adhesive varnish containing non-volatile component 35 % (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone, ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and micro-filler having primary particle size of 12 nm (R974: made by Nippon Aero sol Co.) and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.) were mixed) into the polyimide non-woven cloth of 30 μm; and drying the varnish.

(d) After back grinding the rear plane of the semiconductor wafer 6 to expose the silicon, the above members were adhered to the rear plane of the wafer by heating and pressurizing at 120 ℃ for 5 seconds.

Furthermore, the members were cured by heating at 170 ℃ for 60 minutes.

(e) The via-holes 8 of 50 μm in diameter were formed by YAG laser (made by ESI Co., wavelength: 355 nm, peak power: 4 kW, energy: 200 μj, pulse width: 50 ns).

(f) The conductor portion 9 was formed by injecting conductive paste (GP913: made by Asahi Kasei Co.) into the via-holes 8 by a printing method, and heating and curing at 170 ℃ for 40 minutes.

(g) The external electrode 10 was formed by applying flux at solder ball connecting portions of the substrate 1, whereon the circuit layer was formed, placing eutectic solder ball (Pb 63: Sn 37) of 0.6 mm in diameter thereon, and heating the solder ball by infrared re-flow heating at 240 ℃ for 5 seconds. Finally, marking was performed on the wafer protecting film 7 with an ink jet printer.

In accordance with the above manufacturing steps, the semiconductor wafer 6, whereon plural chip areas were formed as indicated in FIG. 2, was prepared. The amount of warp of the semiconductor wafer 6 was evaluated by film thickness measuring profilometer (dectac: made by ULVAC Co.).

(h) In order to cut the semiconductor wafer 6, dicing tape (UE-111AJ: made by Nitto Denko Co.) was adhered onto the rear plane of the wafer protecting film 7. Then, a dicing saw of 200 μm thick was attached to a dicer (DAD520: made by Disco Co.), and the substrate 1, whereon the circuit layer was formed, the adhesive agent 4, the semiconductor

wafer 6, and the wafer protecting film 7 were cut simultaneously at a same plane so that the semiconductor device 17, obtained by cutting the semiconductor wafer 6, would be an operable smallest unit, i.e. the chip 64. After cutting, the dicing tape was peeled off from the wafer protecting film.

(i) The semiconductor device 17 of the present invention was prepared as explained above. The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in following Table 1.

Table 1

	Amount of warp of wafer(μm)	Amount of warp of package(μm)	Failure generation rate after 1000 cycles*1 (Number of failures/number of tests)
E-1	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-2	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-3	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-4	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-5	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-6	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-7	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-8	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-9	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-10	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
E-11	$\leqq$ 5 μm	$\leqq$ 1 μm	0/100
C-1	-	5 μm	85/100
C-2	-	$\leqq$ 1 μm	20/100*3
C-3	20 μm	5 μm	20/100

*1: Number of breakage failure after 1000 cycles in the range from -55 ℃ to -125 ℃.

*2: Number of failures such as peeling, bubbling etc. during infrared reflow test, after leaving in relative humidity 85 % at 85 ℃ for 166 hours.

*3: Breakage failures between chip/circuit substrate.

*4: Generation of breakage or cracks in chip when dropping from 1 meter high to glass substrate of 5 cm thick was determined as failure.

Table 1 (continued)

	Failure generation rate in reflow test*2 (Number of failures/number of tests)	Failure generation rate in dropping test*4 (Number of failures/number of tests)	Ratio of area (package area/chip area)
E-1	0/100	0/20	1
E-2	0/100	0/20	1
E-3	0/100	0/20	1
E-4	0/100	0/20	1
E-5	0/100	0/20	1
E-6	0/100	0/20	1
E-7	0/100	0/20	1
E-8	0/100	0/20	1
E-9	0/100	0/20	1
E-10	0/100	0/20	1
E-11	0/100	0/20	1
C-1	90/100	0/20	1.44
C-2	0/100*3	8/20	1.2
C-3	50/100	12/20	1

*1: Number of breakage failure after 1000 cycles in the

range from -55 ℃ to -125 ℃.

*2: Number of failures such as peeling, bubbling etc. during infrared reflow test, after leaving in relative humidity 85 % at 85 ℃ for 166 hours.

*3: Breakage failures between chip/circuit substrate.

*4: Generation of breakage or cracks in chip when dropping from 1 meter high to glass substrate of 5 cm thick was determined as failure.

The semiconductor wafer 6 prepared in the present embodiment had a warp as small as equal to or less than 5 μm. The semiconductor device prepared in the present embodiment 17 had a small warp. The conductor portion can be made of a low coefficient of elasticity by connecting the chip 64 to the circuit layer 2 with a conductive resin, and the semiconductor device is made superior particularly in thermal cycle resistance, in addition to the effect of the stress relaxing layer. In accordance with the porous stress relaxing layer, reflow failure in mounting is not generated. The failure such as damage of the chip is not generated in the dropping test. The package size can be made as same as the size of chip. In accordance with the process of the present embodiment, the package can be made only by dicing, and it is superior in mass producibility.

(Embodiment 2)

FIG. 3 indicates manufacturing steps of semiconductor device in the other embodiment of the present invention,

and a semiconductor device obtained by the manufacturing steps.

In accordance with the manufacturing steps of (a) ~ (h), the semiconductor wafer 6 and the semiconductor device 17 of the present invention were prepared.

(a) The porous body 3 made of polytetrafluoroethylene having a three dimensional network structure of 150 μm, which was prepared by a drawing method, the adhesive agent 4, the semiconductor wafer 8 , and the wafer protecting film 7 were arranged as indicated in FIG. 3. The semiconductor wafer 8 of 4 inches in diameter and 525 μm in thickness was used. The adhesive agent 4 and the wafer protecting film 7 were prepared by impregnating the adhesive varnish containing non-volatile component 35 % (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone, ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and micro-filler having primary particle size of 12 nm (R974: made by Nippon Aero sol Co.) and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.) were mixed) into the polytetrafluoroethylene sheet having a three dimensional structure of 30 μm; and drying the varnish. After back grinding the rear plane of the semiconductor wafer 6 so as to remove SiO_2 and to expose silicon, the above members were adhered by heating and pressurizing at 120 ℃ for 5 seconds. Furthermore, the members were cured by heating at 170 ℃ for 60 minutes.

(b) The via-holes 8 of 50 μm in diameter were formed by YAG laser (made by ESI Co., wavelength: 355 nm, peak power: 4 kW, energy: 200 μj, pulse width: 50 ns).

(c) The plated 12 was formed by immersing the semiconductor wafer, wherein the via-holes were formed in the porous body, backed by the wafer protecting film into a plating solution at 70 ℃ to perform an electroless copper plating. Before plating, the semiconductor wafer was immersed into an acidic solution of sensitizer (HS101B: made by Hitachi Kasei Co.)for treating catalyst of catalytic electroless copper plating. The plating solution used had a composition of: copper sulfate heptahydrate; 0.04 mole/liter, ethylenediamine tetraacetic acid dihydrate; 0.1 mole/liter, glyoxylic acid; 0.03 mole/ liter, sodium hydroxide; 0.1 mole/liter, 2, 2'pyridyl; 0.0002 mole/liter, and polyethylene glycol; 0.03 mole/liter.

(d) An etching mask was prepared by applying photosensitive resist (P-RS300S: made by Tokyo Ohka Co.) onto the copper plated film, baking at 90 ℃ for 30 minutes, and exposing and developing the pattern. Then, the copper was etched with ferric chloride aqueous solution (ferric chloride concentration is 40° Baume: specific gravity; approximately 1.38) at 40 ℃, and copper circuit was prepared by peeling off the resist. The circuit 2 was prepared by plating the circuit portion with electrolytic gold.

(e) The solder resist film 13, whereon lands for

external terminals were formed, was prepared using a photosensitive solder resist agent (PSR4000: made by Taiyo Ink Co.) on the circuit 2. The solder resist agent was applied onto the circuit side of the wafer by spin coating method, dried at 80 ℃ for 20 minutes, and exposing and developing to form the lands. Further, it was cured at 150 ℃ for 60 minutes.

(f) The external electrode 10 was formed by applying flux at the land portions, placing eutectic solder ball (Pb 63: Sn 37) of 0.6 mm in diameter thereon, and heating the solder ball by infrared re-flow heating at 240 ℃ for 5 seconds. Finally, marking was performed on the wafer protecting film 7 formed on the rear plane of the semiconductor wafer with an ink jet printer.

In accordance with the above manufacturing steps, the semiconductor wafer 6, whereon plural chip areas 62 were formed as indicated in FIG. 2, was prepared. The amount of warp of the semiconductor wafer 6 was evaluated by film thickness measuring profilometer (dectac: made by ULVAC Co.).

(g) In order to cut, dicing tape 120 was adhered onto the wafer protecting film 7. A dicing saw 11 of 200 μm thick was attached to a dicer (DAD520: made by Disco Co.), and the substrate 1, whereon the circuit layer was formed, the adhesive agent 4, the semiconductor wafer 6, and the wafer protecting film 7 were cut simultaneously at a same plane so that the semiconductor device 17, obtained by cutting the semiconductor wafer 6, would be an operable

smallest unit, i.e. the chip 64. After cutting, the dicing tape was peeled off from the wafer protecting film.

(h) The semiconductor device 17 of the present invention was prepared as explained above. The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment had a warp as small as equal to or less than 5 μm. The semiconductor device prepared in the present embodiment 17 had a small warp, and the semiconductor device is superior particularly in thermal cycle resistance, because the stress relaxing layer is made of porous polytetrafluoroethylene having a low coefficient of elasticity. The semiconductor device does not generate reflow failure at mounting operation, because it is a low humidity absorber. Because the chip can be connected

electrically with the circuit layer by forming the conductors at the via portions and the circuit layer simultaneously by plating, the semiconductor device of the present invention is superior in mass producibility.

The failure such as damage of the chip is not generated in the dropping test. The package size can be made as same as the size of chip. In accordance with the process of the present embodiment, the package can be made only by dicing the semiconductor wafer of the present embodiment, and the process is superior in mass producibility. In accordance with the process of the present embodiment, adjusting locations of the circuit layer and the pads on the chip becomes unnecessary, and the manufacturing process can be simplified.

(Embodiment 3)

FIG. 4(a) and FIG. 4(b) indicate a cross sectional view and a perspective view of the semiconductor device in the other embodiment of the present invention, respectively. The semiconductor device was obtained by the following manufacturing steps.

After forming the via-holes by the same process as the embodiment 2, copper film was formed on the inner wall of the via-holes and the surface of the porous body by a vacuum deposition method. The subsequent processes were performed as same as the previous embodiment to manufacture the semiconductor wafer 6 and the semiconductor device 17.

The semiconductor device 17 was mounted on a mounting

substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment had a warp as small as equal to or less than 5 μm. The semiconductor device 17 prepared in the present embodiment had a small warp, and the semiconductor device is superior particularly in thermal cycle resistance, because the stress relaxing layer is made of porous polytetrafluoroethylene having a low coefficient of elasticity. The semiconductor device does not generate reflow failure at mounting operation, because it is a low humidity absorber. Because the conductive portions are formed by the vapor deposition, the conductive layer having a high purity can be formed, and electrical resistance is decreased. Therefore, the semiconductor can correspond to increasing velocity of electrical signals. The failure such as damage of the chip is not generated in the dropping

test. Furthermore, the package size can be made as same as the size of the chip, and the package can be made only by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 4)

FIG. 5(a) and FIG. 5(b) indicate a cross sectional view and a perspective view of the semiconductor device in the other embodiment of the present invention, respectively. The semiconductor device 17 was obtained by the following manufacturing steps.

As the porous body 3, porous polyimide of 120 μm thick having a three dimensional network structure, which was prepared by a layer transfer method, was used. As the adhesive agent and the wafer protecting film, thermoplastic polyimide (TP-D: made by Kaneka Co.) of 30 μm thick was used, and the semiconductor wafer and the semiconductor device were prepared by the same method as the embodiment 1. However, heating and pressurization for adhering layers was performed at 260 ℃ for one second.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An

appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment had a warp as small as equal to or less than 5 μm. The semiconductor device 17 prepared in the present embodiment had a small warp. The semiconductor device is superior particularly in thermal cycle resistance, because the conductive portions could have a low coefficient of elasticity by connecting the chip to the circuit layer with conductive resin, in addition to the effect of the stress relaxing layer. The semiconductor device does not generate reflow failure at mounting operation, because of the porous stress relaxing layer. The failure such as damage of the chip is not generated in the dropping test. Furthermore, the package size can be made as same as the size of the chip, and the package can be made only by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 5)

The semiconductor device 17, which was the same type as indicated in FIG. 4, was prepared by the following manufacturing steps.

As the porous body 3, porous polyimide of 120 μm thick having a three dimensional network structure, which was prepared by a layer transfer method, was used. As the adhesive agent and the wafer protecting film, thermoplastic polyimide (TP-D: made by Kaneka Co.) of 30 μm thick was used, and the semiconductor wafer 6 and the semiconductor device 17 were prepared by the same method as the embodiment 2.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment has a warp as small as equal to or less than 5 μm. The semiconductor device 17 prepared in the present embodiment has a small warp and superior thermal cycle resistance, and does not generate reflow failure at mounting operation. Because the chip can be connected

electrically with the circuit layer by forming the conductors at the via portions and the circuit layer simultaneously by plating, the semiconductor device of the present invention is superior in mass producibility.

The failure such as damage of the chip is not generated in the dropping test. The package size can be made as same as the size of chip. In accordance with the process of the present embodiment, the package can be made only by dicing the semiconductor wafer of the present embodiment, and the process is superior in mass producibility.

(Embodiment 6)

The semiconductor device 17, which was the same type as indicated in FIG. 4, was prepared by the following manufacturing steps.

As the porous body 3, porous polyimide of 120 μm thick having a three dimensional network structure, which was prepared by a layer transfer method, was used. As the adhesive agent and the wafer protecting film, thermoplastic polyimide (TP-D: made by Kaneka Co.) of 30 μm thick was used, and the semiconductor wafer 6 and the semiconductor device 17 were prepared by the same method as the embodiment 3.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used.

Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment has a warp as small as equal to or less than 5 μm. The semiconductor device 17 prepared in the present embodiment has a small warp and superior thermal cycle resistance, and does not generate reflow failure at mounting operation. Because the conductive portions are formed by the vapor deposition, the conductive layer having a high purity can be formed, and electrical resistance is decreased. Therefore, the semiconductor can correspond to increasing velocity of electrical signals. The failure such as damage of the chip is not generated in the dropping test. Furthermore, the package size can be made as same as the size of the chip, and the package can be made only by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 7)

The semiconductor device 17, which was the same type as indicated in FIG. 5, was prepared by the following

manufacturing steps.

The semiconductor wafer and the semiconductor device were prepared by the same method as the embodiment 1 using alamide non-woven cloth (thermount: made by Du Pont Co.) of 100 μm thick as the porous body 3; and a sheet made of rubber modified epoxy resin of 30 μm thick as the adhesive agent and the wafer protecting film. The adhesive sheet was prepared by applying a varnish (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone, ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and micro-filler having primary particle size of 12 nm (R974: made by Nippon Aero sol Co.), nitrile butadiene rubber (XER-91: made by Nihon Gosei Rubber Co.), and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.) were mixed) onto bed-film, and drying the varnish.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick.

Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment has a warp as small as equal to or less than 5 μm. The semiconductor device 17 prepared in the present embodiment has a small warp. The semiconductor device is superior particularly in thermal cycle resistance, because the conductive portions could have a low coefficient of elasticity by connecting the chip to the circuit layer with conductive resin, in addition to the effect of the stress relaxing layer. The semiconductor device does not generate reflow failure at mounting operation, because of the porous stress relaxing layer. The failure such as damage of the chip is not generated in the dropping test. Furthermore, the package size can be made as same as the size of the chip, and the package can be made only by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 8)

The semiconductor device 17, which was the same type as indicated in FIG. 4, was prepared by the following manufacturing steps.

The semiconductor wafer and the semiconductor device were prepared by the same method as the embodiment 2 using alamide non-woven cloth (thermount: made by Du Pont Co.)

of 100 μm thick as the porous body; and a sheet made of rubber modified epoxy resin of 30 μm thick as the adhesive agent and the wafer protecting film. The adhesive sheet was prepared by applying a varnish (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone, ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and micro-filler having primary particle size of 12 nm (R974: made by Nippon Aero sol Co.), nitrile butadiene rubber (XER-91: made by Nihon Gosei Rubber Co.), and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.) were mixed) onto bed-film, and drying the varnish.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment has a warp as small as equal to or less than

5 μm. The semiconductor device 17 prepared in the present embodiment has a small warp, superior thermal cycle resistance, and does not generate reflow failure at mounting operation. The failure such as damage of the chip is not generated in the dropping test. Furthermore, the package size can be made as same as the size of the chip, and the package can be made only by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 9)

The semiconductor device 17, which was the same type as indicated in FIG. 4, was prepared by the following manufacturing steps.

The semiconductor wafer and the semiconductor device were prepared by the same method as the embodiment 3 using alamide non-woven cloth (thermount: made by Du Pont Co.) of 100 μm thick as the porous body; and a sheet made of rubber modified epoxy resin of 30 μm thick as the adhesive agent and the wafer protecting film. The adhesive sheet was prepared by applying a varnish (biphenyl type epoxy resin (YX-4000: made by Yuka Shell Co.) was dissolved into a solvent, i.e. methylethylketone, ortho-cresol novolak type phenol hardener (H-1: made by Meiwa Kasei Co.) was added, and micro-filler having primary particle size of 12 nm (R974: made by Nippon Aero sol Co.), nitrile butadiene rubber (XER-91: made by Nihon Gosei Rubber Co.), and a catalyst (triphenylphosphine: made by Wako Jyunyaku Co.)

were mixed) onto bed-film, and drying the varnish.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment has a warp as small as equal to or less than 5 μm. The semiconductor device 17 prepared in the present embodiment has a small warp, superior thermal cycle resistance, and does not generate reflow failure at mounting operation. Because the conductive portions are formed by the vapor deposition, the conductive layer having a high purity can be formed, and electrical resistance is decreased. Therefore, the semiconductor can correspond to increasing velocity of electrical signals. The failure such as damage of the chip is not generated in the dropping test. Furthermore, the package size can be made as same as the size of the chip, and the package can be made only

by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 10)

The semiconductor device 17, which was the same type as indicated in FIG. 4, was prepared by the following manufacturing steps.

The porous body portions 15 made of porous polytetrafluoroethylene were adhered to the portions, where the electrodes were not existing on the wafer, of the semiconductor wafer 6 by heating and pressurizing at 120 ℃ for 5 seconds. Simultaneously, the wafer protecting film 7, which was as same as the protecting film in the embodiment 1, was adhered to the rear plane of the wafer. Subsequently, the semiconductor wafer was prepared by screen-printing the photosensitive material portions 14 using the photosensitive resin (BL-9500: made by Hitachi Kasei Co.) onto the electrodes 5 on the wafer, and drying at 80 ℃ for 10 minutes.

After forming the via-holes by exposing and developing the photosensitive portions, curing was performed at 180 ℃ for 2 hours. Subsequently, the semiconductor wafer 6 and the semiconductor device 17 were prepared by the same process as the embodiment 2.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate

FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment has a warp as small as equal to or less than 5 μm. The semiconductor device 17 prepared in the present embodiment has a small warp. The semiconductor device is superior particularly in thermal cycle resistance, because the stress relaxing layer is formed of porous polytetrafluoroethylene having a low coefficient of elasticity, and does not generate reflow failure at mounting operation, because of low humidity absorbing rate. The failure such as damage of the chip is not generated in the dropping test. Furthermore, the package size can be made as same as the size of the chip, and the package can be made only by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 11)

The semiconductor device 17, which was the same type

as indicated in FIG. 4, was prepared by the following manufacturing steps.

The semiconductor wafer was prepared by the steps of: arranging porous body portions made of porous polyimide having a three dimensional network structure of 150 μm, whereon thermoplastic polyimide adhesive layer for adhering to the semiconductor wafer was formed, on the portions of the semiconductor wafer 6, where the electrodes on the wafer were not existing; arranging the anisotropic conductive portions 16 on the electrodes on the wafer using anisotropic conductive film (ASMAT: made by Nitto Denko CO.); and heating and pressurizing. Simultaneously, the wafer protecting film 7 made of thermoplastic polyimide was adhered to the rear plane of the wafer. Subsequently, the semiconductor wafer 6 and the semiconductor device 17 were prepared by the same process as the embodiment 2.

The semiconductor device 17 was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at relative humidity 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount

of warp of the package was also evaluated. The results are indicated in Table 1.

The semiconductor wafer 6 prepared in the present embodiment has a warp as small as equal to or less than 5 μm. The semiconductor device 17 prepared in the present embodiment has a small warp. The semiconductor device is superior particularly in thermal cycle resistance by a synergistic effect with the effect of the stress relaxing layer, because making the conductive portion have a low coefficient of elasticity becomes possible by forming the conductive portion between the chip and the circuit layer with an anisotropic conductive material. The reflow failure at mounting operation is not generated, because of the porous stress relaxing layer. The failure such as damage of the chip is not generated in the dropping test. Furthermore, the package size can be made as same as the size of the chip, and the package can be made only by dicing the semiconductor wafer of the present embodiment. Therefore, the process is superior in mass producibility.

(Embodiment 12)

A cross sectional view and a perspective view of the semiconductor module of the present invention are indicated in FIG. 7 (a) and (b), respectively. The semiconductor module of the present invention was manufactured by the following process.

The semiconductor devices 17 prepared in the

embodiment 1 and the embodiment 2 were mounted on designated portions of a build-up mounting substrate having four layered circuits via flux, and treated for reflow at 240 ℃ for 3 seconds.

The semiconductor module prepared in the present embodiment does not generate any failure at the reflow process in a mounting operation. No failure is generated in the temperature cycle test.

(Comparative example 1)

The semiconductor device indicated in FIG. 8 was prepared by the following process, and evaluated.

After forming the circuit layer by the same method as the embodiment 1, the semiconductor chip 20 was adhered to the circuit layer with die bonding agent 19. Then, the circuit layer was connected electrically to the chip with gold wire 21 using ultrasonic waves. The connecting portion of the chip and the circuit layer was resin-sealed by transfer molding method using an epoxy group sealing agent. Finally, the semiconductor device was completed by forming the external terminals.

The semiconductor device was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at

85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

In case of the present comparative example, the warp of the package is large, because the sealing portion is only on one side of the substrate. Breakage failure is generated in the temperature cycle test, because no stress relaxing layer exists. Reflow failure is generated, because no porous structure for releasing steam exists. The package size becomes larger than the size of the chip, because the chip is connected to the circuit by wire bonding.

(Comparative example 2)

The semiconductor device indicated in FIG. 9 was prepared by the following process, and evaluated.

After forming the circuit layer by the same method as the embodiment 1, a relaxing layer was formed thereon by a printing method using silicone group rubber. A silicone group adhesive agent was applied onto the relaxing layer 23, and the semiconductor chip was adhered. The numerical mark 26 indicates a gold plated lead. After bonding the chip and the circuit layer by ultrasonic waves, the bonding portion was sealed with a silicone group sealing agent 22.

Finally, the semiconductor device was completed by forming the external terminals.

The semiconductor device was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also evaluated. The results are indicated in Table 1.

In case of the present comparative example, breakage failure was generated in the temperature cycle test, because stresses were concentrated to the lead portion connecting the chip and the circuit layer by deformation of elastomer layer during the temperature cycle test owing to using the silicone group material for the stress relaxing layer. Failures such as chip cracks and others were generated by the dropping test, because no protecting film was provided to the rear plane of the chip. The package size becomes larger than the size of the chip, because the lead sealing portion is larger than the chip.

(Comparative example 3)

The semiconductor device indicated in FIG. 10 was prepared by the following process, and evaluated.

Plating bumps 24 are formed at the electrode portions 5 of the semiconductor wafer. Position of the semiconductor wafer is adjusted to match with an epoxy group circuit substrate 25 having the same size as the semiconductor wafer, and the semiconductor wafer is connected electrically to the circuit substrate via the plating bump 24. A liquid epoxy group sealing agent 22 is filled into an interval between the circuit substrate, and the semiconductor wafer, and cured. After forming the external electrodes 10 on the circuit substrate 25, the semiconductor device was prepared by dicing the semiconductor wafer.

The semiconductor device was mounted on a mounting substrate, and a temperature cycle test in the range from -55 ℃ to -125 ℃ was performed. As the mounting substrate, a copper clad glass cloth base epoxy laminate FR-4 (MC-E-67: made by Hitachi Kasei CO.) was used. Furthermore, a reflow test at 240 ℃ for 5 seconds was performed after absorbing moisture in an environment at 85 ℃ and a relative humidity of 85 % for 48 hours. An appearance test such as generation of chip crack and the like was performed after dropping the semiconductor device at a height of 1 meter on a glass plate of 5 mm thick. Furthermore, the package area versus chip area was evaluated. The amount of warp of the package was also

evaluated. The results are indicated in Table 1.

In case of the present comparative example, the warp of the wafer and the package were large, because the protecting film was not provided onto the rear plane of the chip, and failures such as chip cracks and others were generated by the dropping test. Breakage failures were generated in the temperature cycle test, because no stress relaxing film was provided. Failures were generated in the reflow operation, because the sealing portion does not have the porous structure for releasing pressure.

In accordance with the semiconductor devices of the present invention explained in respective of the previous embodiments, the failure generation rate at 1000 cycles is low in comparison with the semiconductor devices of the comparative examples 1, and 3, because the stress generated in the external terminals is small by the presence of the stress relaxing layer. Because the porous body is used as the stress relaxing layer, failure at the mounting reflow is not generated. On account of the presence of the protecting film at the rear plane of the semiconductor chip, the warp of the package is small in comparison with the comparative examples 1 and 3. Furthermore, in comparison with the comparative examples 1 and 3, the failure generating rate by damages, cracks, and the like in the dropping test is small. The package area to the chip area is small in comparison with the comparative examples 1 and 2, because the semiconductor wafer, the stress relaxing layer, and the circuit layer are cut

simultaneously along the same plane to respective units.

The semiconductor device of the present invention comprises a stress relaxing layer between the external terminals and the chip, and an organic protecting film formed on the rear plane of the chip. Therefore, the warp of the semiconductor device is small, and damages at edge portion of the chip and cracks are scarcely generated in the dropping test.

The semiconductor device of the present invention comprises the porous stress relaxing layer between the external terminals and the chip. Therefore, breakage at the external terminals by temperature cycle test after mounting is scarcely generated.

Because the stress relaxing layer comprises a three dimensional network structure, steam generated at the mounting reflow can be released outside the semiconductor device through the core layer, and swelling and breakage of the substrate, whereon the circuit are formed, are seldom generated at the mounting reflow operation.

In accordance with the manufacturing steps of the semiconductor device of the present invention, the package size is as same as the size of the chip, because the assembling operation can be performed simultaneously for the wafer unit. Therefore, the manufacturing method of the present invention is advantageous in mass producibility.

In accordance with the semiconductor wafer of the present invention, the semiconductor device having a high

reliability can be manufactured by mass production. The semiconductor module of the present invention has a high reliability, because the semiconductor device of the present invention is mounted.

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What is claimed is;

1. A semiconductor device comprising:

semiconductor chips,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip.

2. A semiconductor device comprising:

semiconductor chips,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to said stress relaxing layer of said semiconductor chip, and

respective side planes of said stress relaxing layer,

said semiconductor chip, and said organic protecting film are exposed outside on a same plane.

3. A semiconductor device comprising:

semiconductor chips,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

via-holes provided between the electrodes on said semiconductor chip and said circuit layer,

conductive portions for connecting electrically said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern,

an organic protecting film provided on the plane opposite to the plane, where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside on a same plane.

4. A semiconductor device as claimed in any one of claims from claim 1 to claim 3, wherein

said organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of said stress relaxing layer.

5. A semiconductor device as claimed in claim 3, wherein said stress relaxing layer is composed of porous polytetrafluoroethylene.

6. A semiconductor device as claimed in claim 3, wherein said conductive portion in said via-hole is composed of conductive resin.

7. A semiconductor device as claimed in claim 3, wherein said conductive portion in said via-hole is composed of conductor formed by plating.

8. A semiconductor device as claimed in claim 3, wherein said conductive portion in said via-hole is composed of conductor formed by vapor deposition.

9. A semiconductor device comprising:

semiconductor chips,

a porous stress relaxing layer provided on a plane, whereon circuits and electrodes of said semiconductor chip are formed, of said semiconductor chip,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said circuit layer and said electrodes on said semiconductor chip,

external terminals provided at designated portions on said circuits in a grid array pattern,

an organic protecting film provided on the plane

opposite to the plane, where the circuits and electrodes of said semiconductor chip are formed, wherein

respective side planes of said stress relaxing layer, said semiconductor chip, and said organic protecting film are exposed outside on a same plane.

10. A semiconductor wafer comprising:

plurality of chip areas comprising circuits and electrodes, respectively,

a stress relaxing layer provided on a plane, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer, and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to the plane, whereon said stress relaxing layer is provided, of said chip areas.

11. A semiconductor wafer comprising:

plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

via-holes provided between said electrodes and said

circuit layer,

conductive portions for connecting electrically said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the stress relaxing layer of said chip area.

12. A semiconductor wafer as claimed in any of claims 10 and 11, wherein

said organic protecting film has a linear expansion coefficient equivalent to the linear expansion coefficient of said stress relaxing layer.

13. A semiconductor wafer as claimed in any of claims 10 and 11, wherein

said stress relaxing layer is composed of porous polytetrafluoroethylene.

14. A semiconductor wafer as claimed in claim 11, wherein

said conductive portion in said via-hole is composed of conductive resin.

15. A semiconductor wafer as claimed in claim 11, wherein

said conductive portion in said via-hole is composed of conductor formed by plating.

16. A semiconductor wafer as claimed in claim 11, wherein

said conductive portion in said via-hole is composed of conductor formed by vapor deposition.

17. A semiconductor wafer comprising:

plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically said electrodes on said chip area and said circuit layer,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the plane, wherein said circuits and electrodes are formed, of said chip area.

18. A method for manufacturing semiconductor device comprising the steps of:

forming a stress relaxing layer on a plane, whereon circuits and electrodes of respective chip areas are formed, of a semiconductor wafer,

forming an organic protecting film on the plane opposite to the plane, where the electrodes of said respective chip areas,

forming via-holes in said stress relaxing layer on said

chip areas,

forming conductive portions in said via-holes,

forming circuits on said stress relaxing layer,

forming external terminals on said circuit layer, and

cutting said chip areas, the substrate comprising said circuits, and said organic protecting film along a same plane so that the semiconductor device obtained by the cutting becomes a minimum operation unit.

19. A method for manufacturing semiconductor device comprising the steps of:

forming circuit layer on a porous stress relaxing layer,

adhering said stress relaxing layer comprising the circuit layer to a plane, whereon electrodes are formed, of a chip area,

forming an organic protecting film to a plane opposite to the plane comprising said chip area,

forming via-holes in said stress relaxing layer,

forming a conductive portions in said via-hole,

forming external terminals on said circuit layer, and

cutting said chip areas, the substrate comprising said circuits, and said organic protecting film along a same plane so that the semiconductor device obtained by the cutting becomes a minimum operation unit.

20. A semiconductor module mounted with plurality of semiconductor devices as claimed in any one of claims from

1 to 9.

ABSTRACT OF THE DISCLOSURE

Semiconductor devices, semiconductor wafers, and semiconductor modules are provided: wherein the semiconductor device has a small warp; damages at chip edge and cracks in a dropping test are scarcely generated; and the semiconductor device is superior in mounting reliability and mass producibility.

The semiconductor device 17 comprising: a semiconductor chip 64; a porous stress relaxing layer 3 provided on the plane, whereon circuits and electrodes are formed, of the semiconductor chip; a circuit layer 2 provided on the stress relaxing layer and connected to the electrodes; and external terminals 10 provided on the circuit layer; wherein an organic protecting film 7 is formed on the plane, opposite to the stress relaxing layer, of the semiconductor chip, and respective side planes of the stress relaxing layer, the semiconductor chip 6, and the protecting film 7 are exposed outside on a same plane.

FIG.1

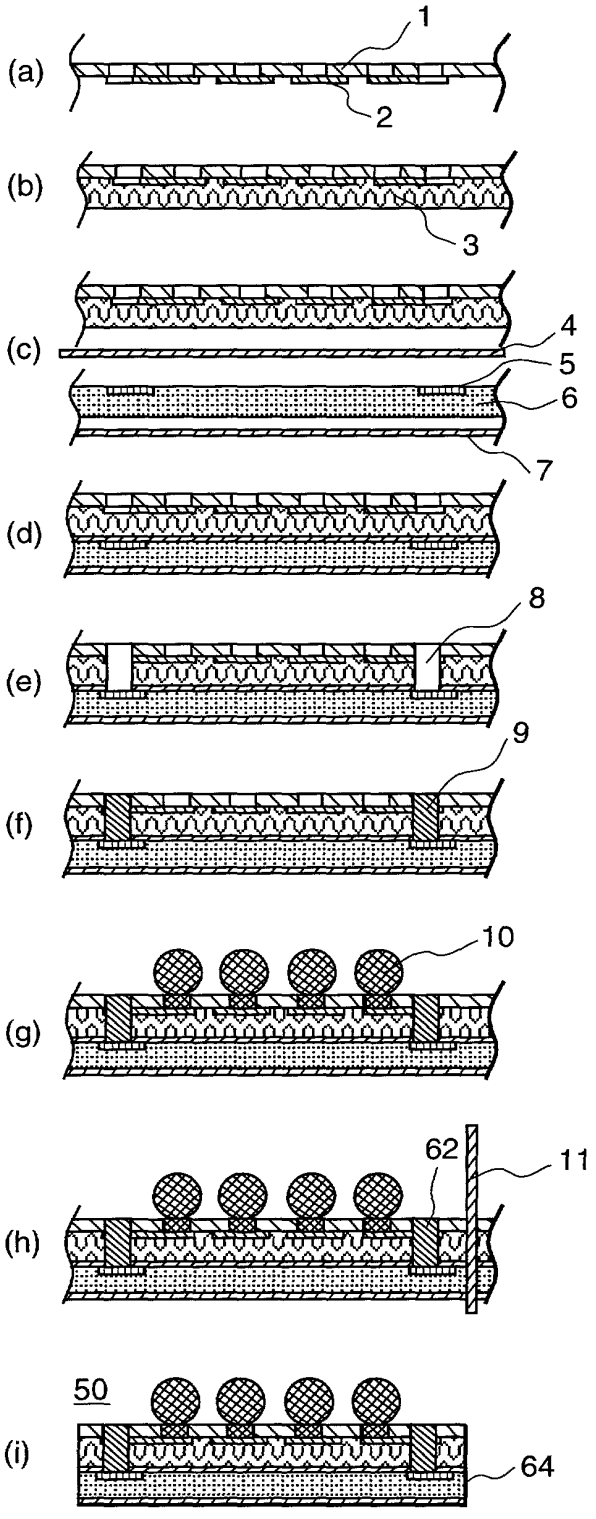


FIG.2

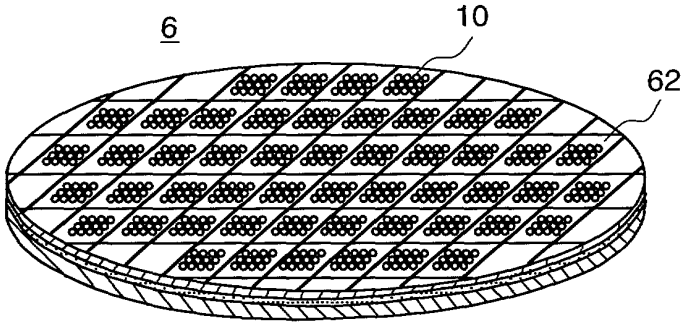
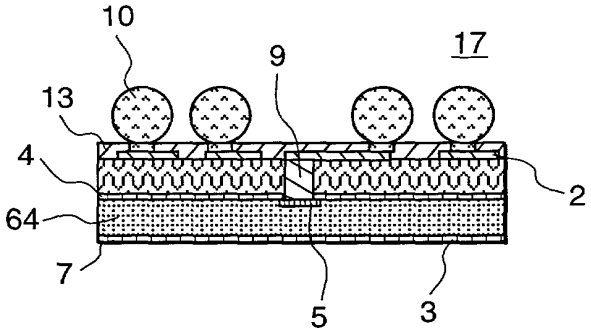


FIG.4

(a)



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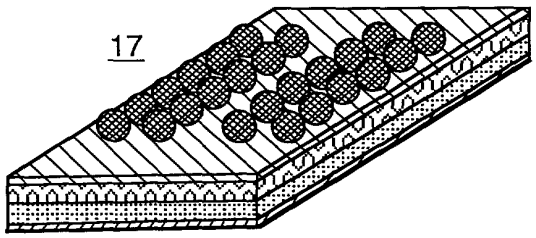


FIG.3

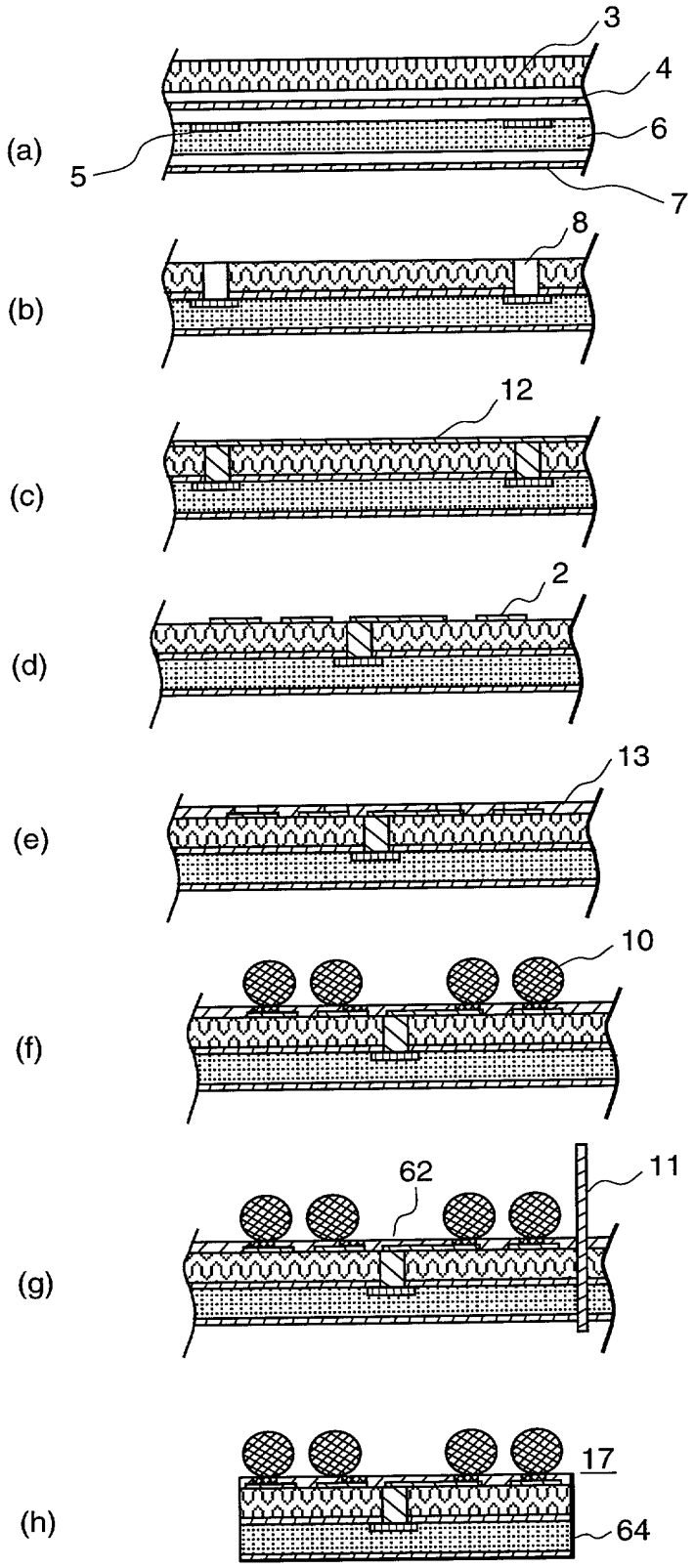
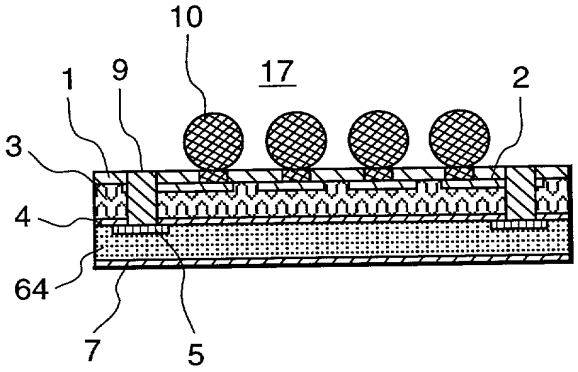


FIG.5

(a)



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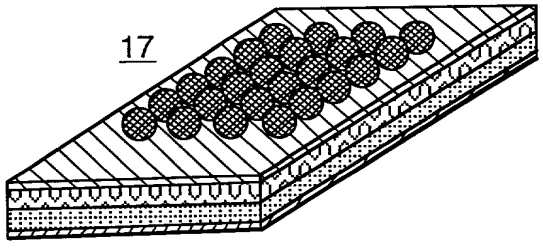
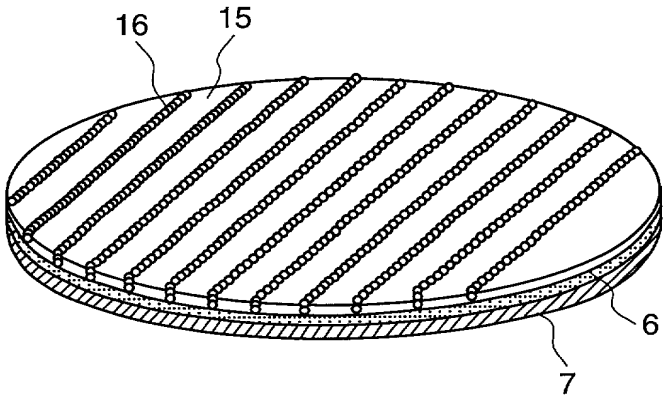


FIG.6

(a)



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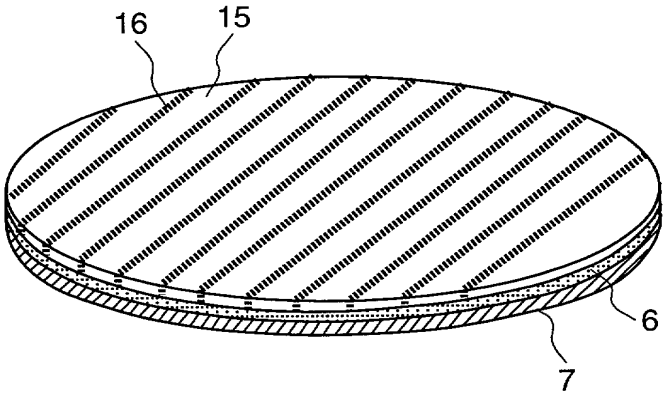

FIG.7

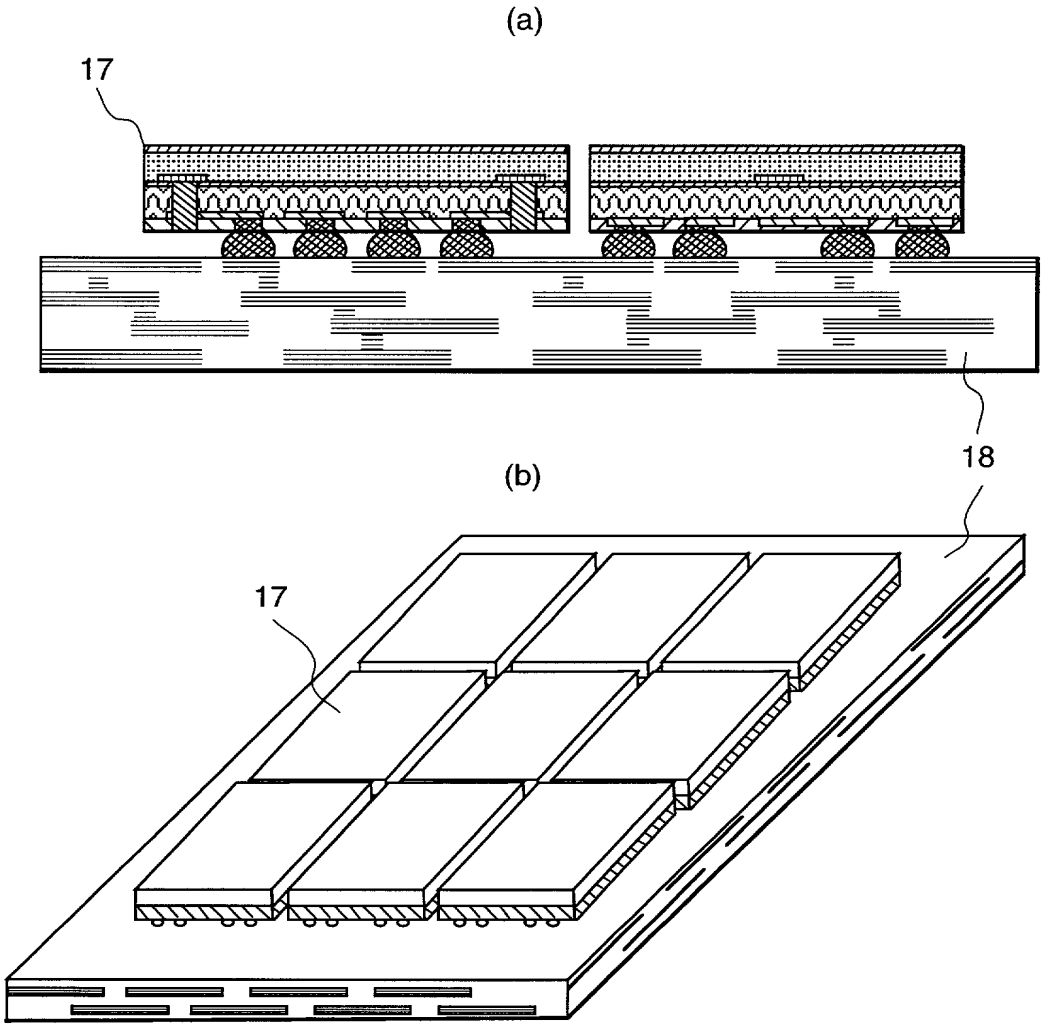

FIG.8

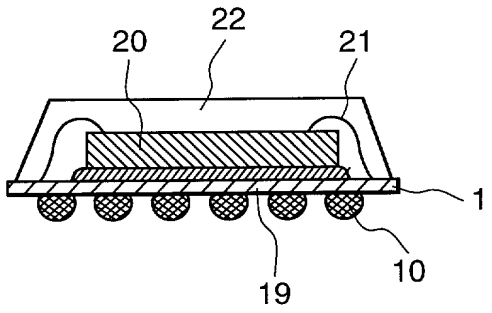

FIG.9

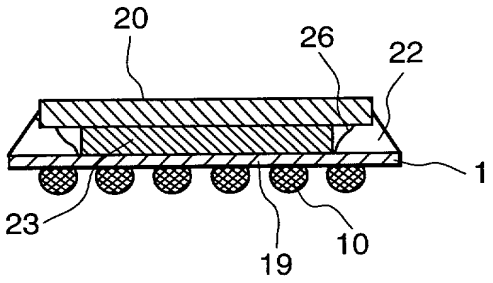

FIG.10

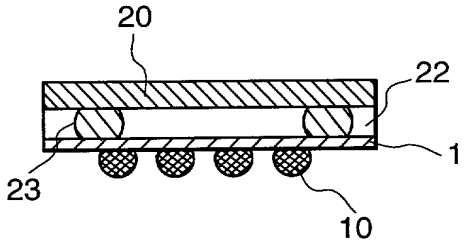

FIG.11